ABSTRACT

A memory circuit has a regular memory cell array; a redundant memory cell array that can replace a failed portion in the regular memory cell array; a redundant replacement memory for storing data on the failed portion in the regular memory cell array; and a pre-charge circuit disposed in the regular memory cell array, depending on the data on the failed portion, the failed portion in the regular memory cell array is replaced with the redundant memory cell array, whilst a pre-charge path is closed which leads to the pre-charge circuit corresponding to the failed portion. This enables a common redundant replacement memory to effect a relief of the failed portion and shutoff of the pre-charge current to the failed portion.